

REMARKS

The amendments to the claims are responsive to the Board's opinion mailed August 22, 2003. Summarizing, the Examiner took the position, and the Board agreed, that the recitation of "a multiple gate transistor structure" as recited in appealed claim 15, a representative pending claim, was not expressly limited to a structure comprised of a single transistor having multiple gates. Based upon this broad interpretation, the Examiner cited and relied upon U.S. Patent No. 4,319,263 (Rao '263), which teaches a structure whereby adjacent transistors, each having a single gate, share a common source/drain region.

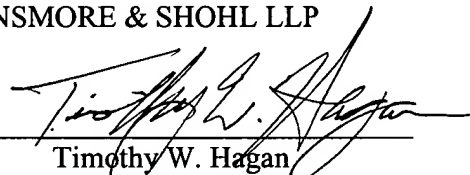
An embodiment of the present invention includes a conductive spacer formed partially over the gate. The conductive spacer is contacted and driven separately from the gate, defining a multiple gate transistor. By using the conductive spacer as a gate, turn off of the transistor may be ensured by supplying a negative voltage on the conductive spacer. Notably, the gate and the conductive spacer gate cooperate to open or close the channel between source and drain regions of a single transistor device. This is quite different than the structure taught in Rao '263, where transistors are formed such that adjacent transistors share either a common source or drain region and are constructed such that the gates of the adjacent transistors partially overlap. Rao '263 does not teach or suggest the presently-claimed structure recited in amended claims 15-23 and newly-added claim 33.

Early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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